Dual-Band/Tri-Mode Receiver IC for N- and W-CDMA Systems Using 6''-PHEMT Technology

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***Abstract* — A dual-band/tri-mode receiver IC for CDMA based mobile systems has been fabricated using our 6''-PHEMT production line, comprising the complete RF front end and one IF stage. The first LNA stage exhibits an input IP3 of +8 dBm and a noise figure of 1.0 dB, the overall gain of the complete receiver is 26.0 dB. The current consumption only is 17 mA, for a minimum LO power demand of –7 dBm.**

I. Introduction

The continuous development and implementation of more sophisticated wireless phone systems results in the coexistence of various systems in all regions of the world. Although the scheduled W-CDMA systems throughout the world, such as CDMA2000 or UMTS, evolve being more compatible to each other, each of them still accounts for local particularities of mobile phone markets in terms of features and use of the phones. Therefore the market demands components which allow operation in various frequency bands and in different phone systems. However, with the availability of higher data rates and more economic distribution of bandwidth adapted on the individual requirements of each subscriber, the frequency spreading is further increased and results in higher linearity requirements of all components. Usually an improved intermodulation performance is achieved by driving more current through the devices. At the same time, when phone manufactures step forward to their next generation, they usually reduce the number of components and board area and at maximum keep up the overall current consumption.

For the aforementioned reasons, a market pull to the use of more sophisticated device technologies, either SiGe [1] or GaAs based HBTs or GaAs based HEMTs, can be observed. Independent of the choice of material, compared to the conventional MESFET or Si based devices those technologies are more complex, requiring either more mask levels or epitaxial material. The HEMT is famous for its excellent intermodulation characteristics, even for low current densities, and its low noise figure. Whereas this device used to be optimized in terms of f_T and f_{max} for high frequency applications even by use of e-beam lithography, for high volume markets a production ready and cost-effective technology is needed. With Infineon Technologies, based on a millimeter-wave HEMT process [2] a cost-effective HEMT process has been established, using optical gate lithography in conjunction with a spacer process. The device with a gate length of typically 0.4 µm exhibits a threshold voltage of –0.3 V and a maximum current densitiy of 500 mA/mm. Furthermore, for high volume manufacturing, this technology has been transferred to 6''-epitaxial wafers, resulting in an increased wafer area by a factor of 2.5.

II. Design Features of the Receiver IC

The IC incorporates two independent RF receiver chains, as can be seen in the block diagram in Fig. 1. Each chain comprises two LNA stages, out of which the first can be bypassed, and a mixer block consisting of a resistive FET mixer with an LO buffer [3]. For suppression of TX leakages and image rejection, a 50Ω bandpass filter can externally be connected between the two LNA stages. For either RF chain, one of two IF amplifiers can be selected, depending on the gain, current and filtering requirements of different systems.

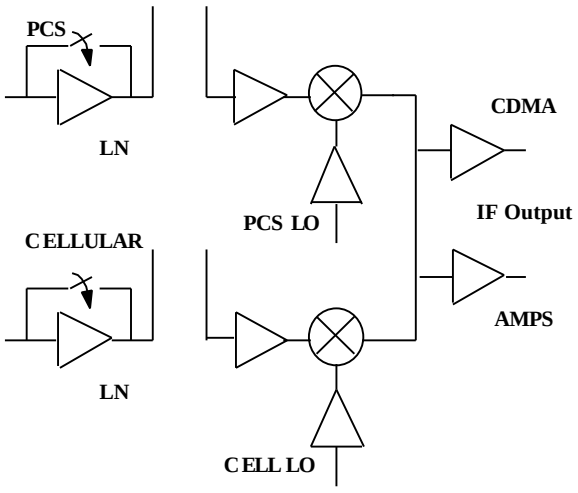

Fig. 1. Block diagram of the dual-band receiver IC.

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Each chain can be operated in three gain/current modes. In the high gain mode, both LNA stages run for maximum gain and linearity and minimum noise figure. In the reduced current mode (e.g. RX Only), both RF stages are lowered in current while the gain remains nearly the same as in the high gain mode. Finally a low gain mode is available, where the first LNA stage is switched off and bypassed to increase the maximum input power capability with significant current savings. The device requires only positive supply and control voltages for switching off inactive gain stages, no external switching transistors are required.

Both receive chains can independently be tuned for different frequencies. In our first approach, the upper chain was optimized for use in PCS N-CDMA systems (IS-95), whereas the lower band was designed for cellular N-CDMA and AMPS systems. PCS and cellular N-CDMA share the IF amplifier whereas AMPS employs a separate IF amplifier, accounting for the different gain requirements. As an alternative, only by changing some air bridge options in the last metallization layer, the upper chain can be adapted for W-CDMA systems (CDMA2000, UMTS), operating at 2.15 GHz.

The die is incorporated into a leadless 24-pin package of 3.5 x 4.5 mm² size and a height of 0.9 mm, called VQFN-24.

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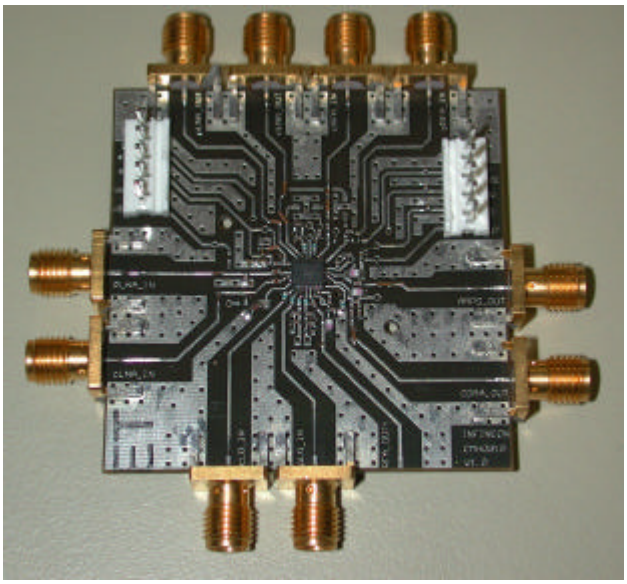

Fig. 3. Photograph of the demonstration board of the dual chain receive IC; dimensions: 50x 50 mm².

III. MEASURED PERFORMANCE FOR N-CDMA

The packaged device was soldered on an FR4 board and assembled for application in cellular and PCS N-CDMA systems (IS-95) and for AMPS. A schematic diagram and a photograph of the demonstration board are depicted in Fig. 2 and Fig. 3, respectively.

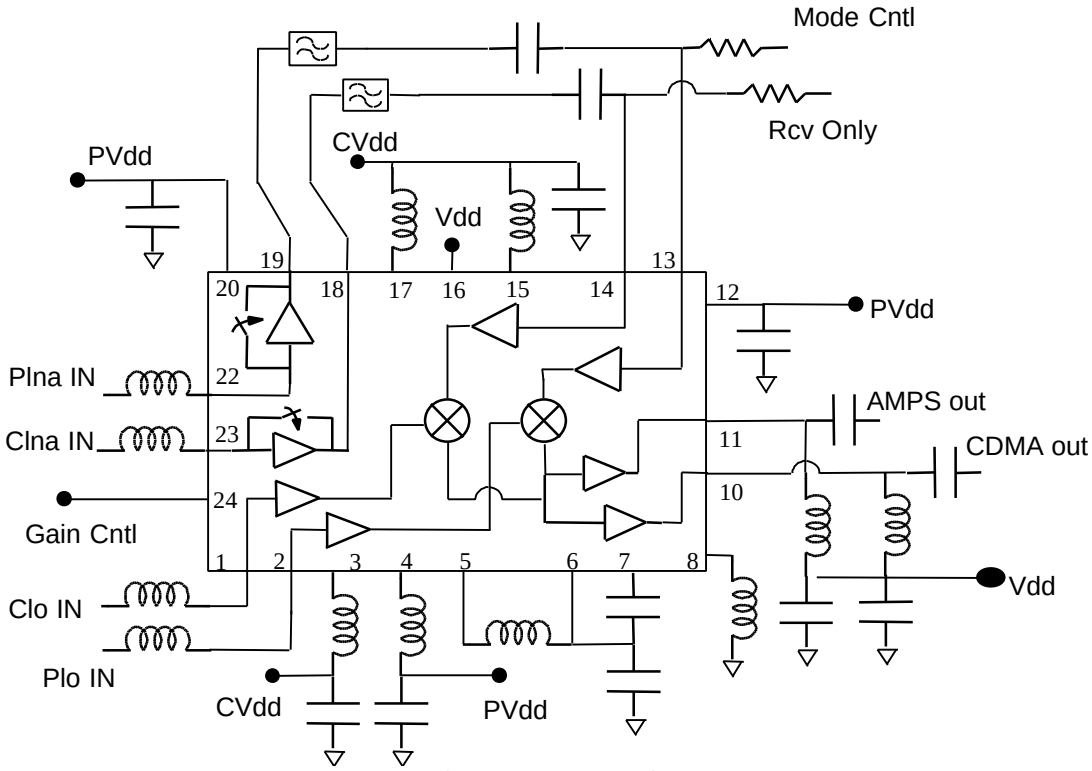

Fig. 2. Schematic of application circuit of dual-band receive IC.

For fully functional operation, the IC requires 29 external passive components. All parameters shown below are measured by means of this demonstration board. Similar performance of all significant RF parameters was achieved for cellular and PCS N-CDMA band.

A. First LNA stage

In Fig. 4 and in Fig. 5, S-parameters and noise figure, respectively, are shown for the first LNA stage in high gain mode for PCS band. From 1930 to 1990 MHz, the gain is 12 dB and the noise figure is lower than 1.0 dB. The current consumption of this stage is 5 mA. In the low gain mode, this LNA stage is bypassed to increase the maximum power capability, resulting in a gain of –6.5 dB in the full band. The S-parameters in the low gain mode are shown in Fig. 6. It is important to note that for both gain modes the same external components are used and independent of the gain mode, input and output return loss

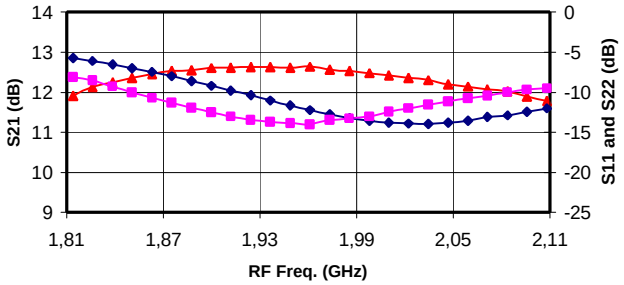

Fig. 4. S-paramaters of the first LNA stage in high gain mode.

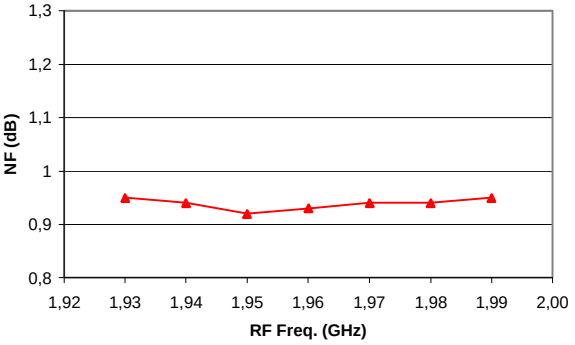

Fig. 5. Noise figure of the first LNA stage in high gain mode.

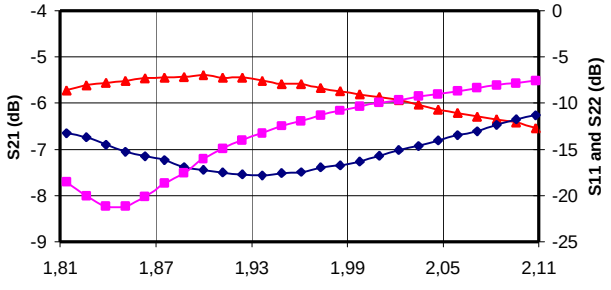

Fig. 6. S-parameters of the first LNA stage in low gain mode.

are better than 10 dB. The input 3rd order intercept point is 8 dBm in high gain and 25 dBm in low gain mode, respectively. Depending on system and customer requirements, gain and current can be tuned over a wide range to optimize overall linearity requirements.

LNA, 1st stage	High Gain	Reduced Current	Low Gain
Gain [dB]	12.5	12	-6
NF [dB]	1.0	1.2	6
IIP3 [dBm]	8.0	5.0	25
Iop [mA]	5	3	0

Tab. 1. Performance summary of first LNA stage of receive IC (both cellular and PCS).

B. Down-Converter Performance

The RF amplifier preceding the mixer establishes a very low noise figure for the down-converter section when compared to competing SiGe solutions. The IC can accommodate either high or low side LO frequencies and allows IF frequencies from 50 to 400 MHz. For cellular operation the minimum LO power is –10 dBm, while the PCS converter requires –7 dBm. Gain in the CDMA IFA can be adjusted externally. Table 2 summarizes the down-converter performance.

Down-converter	High Gain	Reduced Current	AMPS
Gain [dB]	17	16.0	13
NF [dB]	4.1	4.3	5.5
IIP3 [dBm]	+ 0.5	-1	0
Iop [mA]	12	11	10

Tab. 2. Performance summary of down-converter section of receive IC (both cellular and PCS).

C. Overall Performance

The overall performance is affected by the properties of the external filter between the two LNA stages. The overall performance has been investigated including a SAW filter with a loss of approximately 3 dB. As an example,

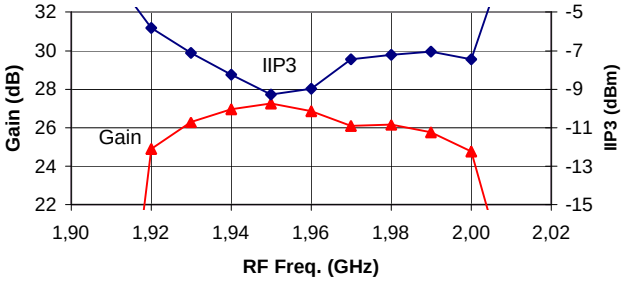

Fig. 7. Overall Gain and IIP3 of PCS receiver in high gain mode with filter (PCS band).

LNA/Down-converter CDMA (PCS)	High Gain	Reduced Current	Low Gain
Gain [dB]	26.0	24.5	8.5
NF [dB]	1.8	2.0	12.5
IIP3 [dBm]	-9.0	-10.0	+ 9
Iop [mA]	17	14	12
LNA/Down-converter AMPS			
Gain [dB]		22.0	
NF [dB]		2.1	
IIP3 [dBm]		-6.0	
Iop [mA]		14	

Tab. 3. Performance summary of dual-band/tri-mode receiver IC, for an LO power of –7 dBm (including filter).

again the PCS performance will be shown, since it can be considered more critical compared to the application in cellular bands.

The RF performance of the different gain modes in the PCS band is summarized in Table. 3. For the full band, gain and input IP3 are shown in Fig. 7. In the high gain mode, for an LO power as low as –7 dBm, the overall gain of the complete receiver line-up is 26 dB, the input IP3 is –9.0 dBm, resulting in an output IP3 of 17 dB. The total noise figure is less than 1.8 dB with a total current consumption of only 17 mA. To the authors knowledge this is the lowest current consumption for a complete receiver line-up of a CDMA mobile phone reported so far, independent of the device technology.

IV. MEASURED PERFORMANCE FOR W-CDMA

For one chip variant, the high frequency band was optimized for W-CDMA applications at 2.15 GHz. The performance over the frequency band from 2.12 to 2.18 GHz for high side injection with an IF of 190 MHz is depicted in Figs. 8 and 9. For the LNA, a gain of 12.5 dB with a noise figure of 1.1 dB was achieved for a current of 7 mA. Its IIP3 was nearly 10 dBm. For the down-converter, the conversion gain was 17 dB with an IIP3 of +2 dBm, running at a current of 14 mA and an LO power of –3 dBm.

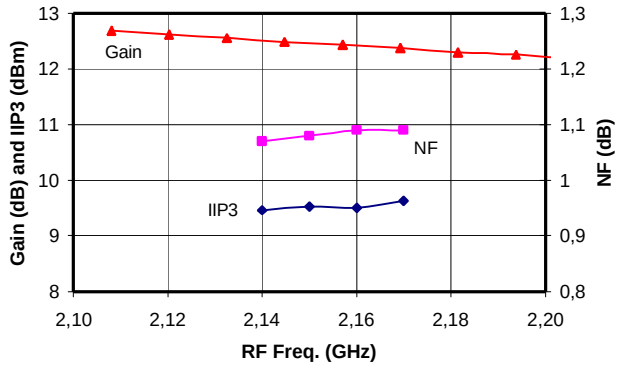

Fig. 8. Gain and IIP3 of W-CDMA LNA.

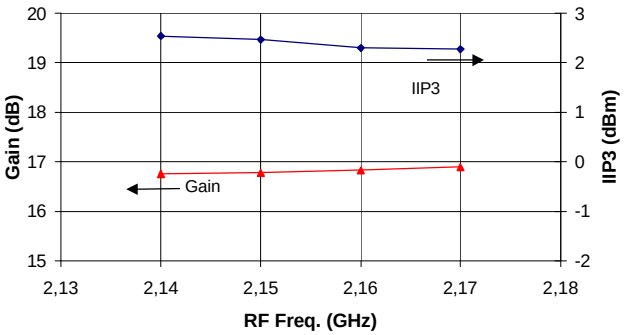

Fig. 9. Gain and IIP3 of W-CDMA down-converter.

V. CONCLUSION

The linearity requirements for the up-coming mobile phone systems pull the exploitation of more sophisticated technologies. By use of a PHEMT technology, Infineon Technologies has achieved a dual-band tri-mode receiver MMIC with state of the art noise figure and linearity performance. In addition, the IC's package size is only 3.5 x 4.5 mm which is smaller than any competing solution. Showing 1.0 dB noise figure, 12.5 dB gain and 8 dBm IIP3 for the LNA, and having 17 dB gain, 0.5 dBm IIP3 for the down-converter, with a total current consumption of only 17 mA, the device meets the linearity requirements of both N-CDMA and W-CDMA systems. Even higher IIP3 can be achieved by modestly increasing the current consumption. To the authors' knowledge, this dual-band/tri-mode receiver establishes a new benchmark for low current consumption and RF performance in a production ready MMIC exceeding the requirements of CDMA handsets.

REFERENCES

[1] J. Imbornon et al., "Fully Differential Dual-Band Image Reject Receiver in SiGe BiCMOS", *2000 IEEE RFIC Symposium Dig.*, pp. , June 2000.

[2] J.-E. Müller et al., "A GaAs HEMT MMIC Chip Set for Automotive Radar Systems Fabricated by Optical Stepper Lithography," *IEEE Journal of Solid-State Circuits*, vol. 32(9), pp. 1342-1349, 1997.

[3] H. Banzer and M. Poebl, "Ultra High Linear GaAs Mixer CMY210," *Microwave Journal*., pp. 354-360, May 2000.